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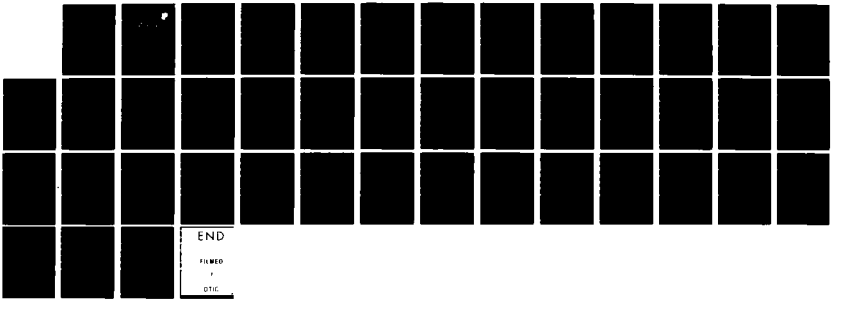

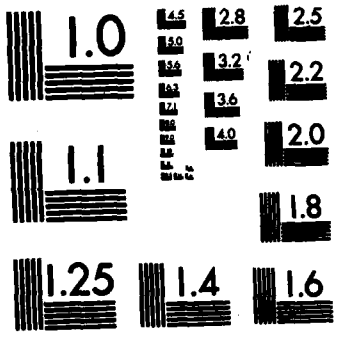

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Interim Report
December 1982

"INVESTIGATION OF CHARACTERISTICS AND APPLICATIONS OF NEW CCD SIGNAL PROCESSING DEVICES"

Northeastern University

Basil L. Cochrun
John G. Proakis

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes work aimed toward the development of two high speed sampled analog signal processing modules based on charge coupled device (CCD) technology. The modules will be controlled by a Z-80 microprocessor. The report provides an overview of the microprocessor software development efforts, a description of the circuitry for the refreshable sampled analog memory (RSAM), a functional description of the interface board designed for transferringdata from the microprocessor to the CCD modules

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and the analog signal generator.

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1. Introduction

The objective of this program is the development of two high speed sampled analog signal processing modules based on charge coupled device (CCD) technology. The modules will be controlled by a microprocessor. Under program control, each module will have the capability of performing a number of sampled analog signal processing functions.

One signal processing module will handle sampled analog line data. That is, it will be capable of computing quantities of the form

$$y_k = \sum_{n=1}^{N} a_{k-n}\, b_n \quad ,$$

where the sequence $\{a_n\}$ represents a set of N samples of the input signal and $\{b_n\}$ represents a reference vector consisting of N points. This type of computation is encountered in performing correlation, filtering and synchronization. In addition, the module will have the capability of performing integration. The second signal processing module will handle two-dimensional, array-formatted data. That is, it will be capable of performing two-dimensional signal processing operations such as filtering, correlation and Fourier transforms.

The general configuration for the sampled analog signal processing system under development is illustrated in Figure 1.1. The CCD signal processing module is controlled by the microprocessor through a digital interface. In order to demonstrate

that the CCD signal processor is performing its specified functions, it is necessary to also implement an analog signal generator which provides the analog input to the CCD signal processing module. The microprocessor is programmed to control the signal generation in the analog signal generator. Noise may be added to the signal from the signal generator and the combined signal is the input to the CCD signal processing module.

The microprocessor selected to serve as the controller is the Zilog Z-80. For the development of software, the microprocessor was augmented with a dual-floppy disk and a DECWRITER IV terminal.

There are two CCD's that have a digital interface and, thus, lend themselves to microprocessor control. One is an analog/binary correlator (ABC) which is a 512-tap (transversal) delay line with 1-bit (± 1) digitally controlled tap weights. The second device is a programmable transversal filter (PTF) which consists of eight 128-tap delay line sections that may be interconnected in nine different modes. The 1-bit tap coefficients and the mode are digitally selected. Thus, the tap coefficients for the ABC and the PTF and the mode for the PTF can be controlled by means of the microprocessor.

In order to interface the microprocessor to the ABC and the PTF, it is necessary to design and construct interface circuitry. This circuitry was designed and mounted on a single printed circuit board that is connected to the microprocessor chassis. A direct memory access (DMA) device is used for the purpose of

achieving high speed data transfer from the microprocessor to the PTF and the ABC. The DMA is also used to transfer the digital signal from the microprocessor to the input of the signal generator. A functional block diagram of the system is shown in Figure 1.2.

In addition to the ABC and the PTF, there are two other sampled analog CCD's that have no programmability features. One is a 512-stage refreshable sampled analog memory (RSAM) and the second is a 32 x 32 cell corner turning memory (CTM). The only potentially interesting connection between these devices and the microprocessor is to feed the output of each device back to the microprocessor via an A/D converter.

The ABC, PTF, RSAM and CTM were provided as GFE. In addition to these devices we purchased two RETICON boards which employ a pair of CCD transversal filters to perform a discrete Fourier transform via the chirp Z-transform algorithm. The line formatted CCD module and the array formatted (two-dimensional) CCD module are to be configured from interconnection of these basic CCD building blocks.

This interim report describes our work on the software development for the microprocessor, the hardware for the RSAM and the DMA interface board.

2. Software Development for the Z-80 Microprocessor

The Z-80 microprocessor configures and controls the signal processing module. It is also a source of selectable test data to exercise the various CCD's mentioned in the previous section.

In this section we give an overview of the software development work and describe the software for the PTF. Listings of computer programs are not included in this interim report. These will be provided in the final report on this contract.

Overall Software Framework

Most of the programming has been done in FORTRAN. This was not our original intention. Our first thoughts were that all programming would be in assembly language and that control and modification would be through the debugging software. We thought this would be necessary to realize the speed and memory economics required.

However, very few activities demand great speed or tight coding. For those that do, e.g., generation of maximal length shift register sequences, DMA (Direct Memory Access) control from Z-80 memory to the D/A converter, we programmed in assembly language. The larger part of the programming is for set-up. This requires interrogation, parameter selection and data transformation to enable the initializing and loading of the signal processing system components. Besides, once used these programs can be overlaid with newer programs until needed again at a later time.

There was, of course, the matter of interfacing the FORTRAN and assembly programs. There were some initial problems, system software and system documentation being somewhat lacking in capability and correctness. These obstacles have been overcome.

Benefits of Software Framework

The benefits of our approach are principally:

1. Easier interactive operator control.
2. Avoidance of some assembly language housekeeping functions --
   a. stack register set-up
   b. load point selection
   c. etc.
3. Availability in FORTRAN of almost all logical operations present in assembly language.
4. Ability to manipulate F-bit byte variables.
5. Easier linking of main and subroutines.

Some minor benefits are surrendered when adopting the FORTRAN framework. Whereas working under control of the object time debugger affords the programmer access to each memory location and the ability to set breakpoints at any instruction, this FORTRAN has no such non-invasive debugging accessories. To overcome this we wrote some binary and hexadecimal print-out routines. Since these are subroutines they are easily invoked and their removal from a running program is no trouble.

Programmable Transversal Filter Software

The programmable transversal filter (PTF) configuration requires the mode and constants as parameters. One mode treats the constants as 1024 1-bit numbers, Mode 1, where these bits are a portion of or the entire length of a maximal length sequence. For that requirement we programmed a general purpose assembly language module that can generate any such sequence up to length

$2^{31} - 1$. Both the tap positions and the initial state of the shift register are selectable by the operator.

However, once the sequence is generated it is not in a form for immediate loading into the filter. The bits must be fed serially into the constant register and further, depending on the programmable filter mode, require a particular order in which the bits are received for storage. We have written a generalized routine that will transform the filter coefficients, as a function of the filter mode, for correct loading.

When testing the PTF for correlation with the 1024 by 1-bit coefficients the D/A converter in the analog signal generator is fed the same random sequence. Because of the hardware design there must be a remapping of the data. The choice was one of complicating the hardware or putting the burden on the software to accomplish the simple transformation. Our decision was to go with the software solution for an easy solution. This program is completed.

The D/A converter in the analog signal generator operates on 2's complement 8-bit integers. To test its performance and the ability to load it continuously there is a FIFO (first-in, first-out) hardware stack that must be filled on demand from the Z-80 memory. This is an assembly language subroutine that is callable from FORTRAN. Two simple functions, a ramp and a sine, have been successfully tested as inputs to and outputs from the D/A.

Total System Test

A FORTRAN main program using the required subroutines has been written to test the system operation for the PTF in Mode 1. Since the filter has not yet been delivered we could only test to see if the various signals and set-up states were operating properly. This routine will be made more general in enabling the user to select filter modes and data to be processed. This effort will be largely organizing the tools we have already completed. Some design work and some programming has been completed.

Engineering Aids

The system architecture has the hardware devices hung on the bus and thus addressable by the Z-80 software. When testing the hardware modules as they were completed it occurred to us that software might be able to afford a flexible testing tool. A simple interactive tool permits the engineer to do the following:

1. Select an output port address in hexadecimal.
2. Select an 8-bit byte of data, as two hexadecimals, or a ramp function to be sent to the address selected in Step 1.
3. Specify the number of times (up to 30,000) that the data is to be sent to that port.
4. Repeat Step 1 through Step 3 automatically.
5. Reset Steps 1 through 3 with new parameters.
6. Exit to the Z-80 monitor.

This seemingly primitive program, written in FORTRAN, has been extremely helpful in validating our hardware and in finding

hardware errors.

3. Refreshable Sampled Analog Memory (RSAM)

Introduction

The RSAM is a low loss CCD delay line with the closed-loop race track geometry shown in Figure 3.1. RSAM TC 1230A is a 1024-stage CCD capable of storing and circulating 512 signal samples. RSAM TC 1230B is a 256-stage CCD capable of storing and circulating 128 signal samples. Each RSAM has provision for signal addition to any signal samples already circulating in the loop. Figure 3.1 shows the basic structure for the 1024-stage CCD. The 256-stage CCD differs from the 1024-stage in that it has only a single refresh stage. Details of the physical structure and operation of the RSAM have been documented by W. F. Kosonocky and D. J. Sauer in an interim RADC report [1].

The RSAM has both destructive and non-destructive readout. In Figure 1 these are shown as DRO and NDRO respectively. The DRO output port is a floating diffusion structure which is used to remove signal charge from the CCD loop. The two NDRO ports are floating gate structures which are useful for evaluating transfer efficiency without disturbing the circulating signal charge.

Provision is made for two inputs, as indicated in Figure 3.1, the input signal charge and the trailing bias charges. Signal strobe pulses, S_{2A}, occur during even clock cycle times and trailing bias charge strobe pulses, S_{1B}, occur during odd clock cycle times. Low loss operation is directly attributable

to this input capability where a large trailing bias charge can be inserted in the loop between each signal charge packet. Transfer efficiency is improved by periodically recombining the signal charge transfer losses collected by the trailing wells with the corresponding signal charge packets in the refresh stages.

The RSAM available time delay is several orders of magnitude larger than that for conventional CCD's. This is accomplished by means of the dark current subtraction stages which periodically remove fixed amounts of dark current generated charge.

Circuit Partitioning

In the interest of flexibility for testing and interchanging of chips the RSAM system structure is modular making use of two TM 506 power modules with Option-02. Figure 3.2 indicates the modular arrangement using standard single and double bins. Bin RS-1 contains the most critical bias supplies and controls, i.e., the ones requiring adjustment most often, and especially so when chips are interchanged. Bin RS-2 houses a DVM and the less critical bias supplies and controls. Double Bin RS-3 contains the digital and analog circuits on separate boards.

Circuit Details

(a) Master Clock (MCK)

The MCK circuit is shown in Figure 3.3. It consists of a crystal oscillator with square wave TTL level output and 50% duty cycle.

The crystal frequency is divided down by 2^n, where n = 1 - 8, giving RSAM input clock frequencies from MCK/256 to MCK/2. Power

for the MCK circuitry is derived from the internal power available from the TM 506 using a μA 7805 regulator.

(b) RS-3 Digital Board

The RSAM requires a two-phase clock for the CCD loop gates running at half the rate of the MCK, or $MCK/2^{(n+1)} = CK$. The two phases are designated as ϕ_1 and ϕ_2. $\overline{\phi}_1$ and $\overline{\phi}_2$ at TTL levels are generated by dividing the input $MCK/2^n$ by 2 using the D-type flip-flop IC_2 pins 8, 12. CK is inverted by IC_4, pin 3, giving $\overline{\phi}_2$. $\overline{\phi}_2$ is inverted by IC_7, pin 2, giving $\overline{\phi}_1$. The circuitry is shown in Figure 3.4a. $\overline{\phi}_1$ and $\overline{\phi}_2$ are then inverted and translated to variable amplitude clock waveforms using MH0026 driver amplifiers located on the analog board in RS-3. The remainder of the timing pulses, synchronized with CK or $\overline{CK}$, shown in Figure 3.4a and 3.4b are required for read-in, read-out and circulation time for the CCD loop.

$\overline{CK}$ at pin 9 of IC_2 is divided down by IC_8 through IC_{12} to obtain LOOP SIZE and TOTAL DELAY pulses. In Figure 3.4b the LOOP SIZE switch is shown in the 256 position with the signal obtained at pin 14 of IC_{10} at a frequency of $CK/2^9$. The pulse width of this signal corresponds to the length of the CCD loop, i.e., 256 clock cycles. The TOTAL DELAY signal period determines the overall cycle time, i.e., the number of CCD loop cycles. A simplified timing diagram for the 256-stage closed-loop CCD for the switch positions shown in Figure 3.4b is shown in Figure 3.5.

The leading edge of the TOTAL DELAY signal initiates LOOP CYCLE N during which $\overline{\phi}_{FDT}$ is pulsed 256 cycles which reads out

the charge stored in the CCD loop via the floating diffusion output stage, shown as DRO in Figure 3.1. During this readout time $\overline{\phi}_{REC}$, loop circulation clock signal, is inhibited. At the end of the readout interval LOOP CYCLE "0" is initiated. $\overline{\text{GATE B}}$ goes low activating the strobe pulses S_{1A} and S_{1B} as indicated in Figure 3.4a. After 128 pulses of S_{1A} and S_{1B}, during which time input signal and trailing bias charges are introduced into the CCD loop, $\overline{\text{GATE B}}$ goes high and remains high until after the next leading edge of the TOTAL DELAY signal.

The remaining clock signals shown in Figure 3.4a are: $\overline{\phi}_{BC}$, ϕ_{RG}^{-}, S/H, $\overline{DCS_1}$, $\overline{DCS_2}$, ϕ_{FG}^{-} and ϕ_{R}^{-}. ϕ_{BC}^{-} is the clock for regeneration of the trailing bias charge. Its frequency is the same as $MCK/2^n$ or twice that for CK. ϕ_{RG}^{-} is the clock for combining the signal and trailing bias charges, referred to as refresh ports in Figure 3.1. ϕ_{RG}^{-} is generated by gating the CK pulse with the output of D-type flip-flop IC_2 pin 6 which has twice the CK period. The last four signals are all derived from the dual monostable flip-flop IC_5 with provision for adjustable pulse widths and synchronized with CK. $\overline{DCS_1}$ and $\overline{DCS_2}$ are clocks for the dark current subtraction stages. The frequency can be either at the CK rate or $\frac{1}{2}$ CK depending on whether the input of IC_6 pin 1 is at +5 volts or at the output of IC_2 pin 6 respectively. ϕ_{FG}^{-} and ϕ_{R}^{-} are clocks for the floating gate and floating diffusion reset gates respectively.

(c) RS-3 Analog Board

The TTL level signals originating on the digital board in

RS-3 are all inverted translated to the necessary clock amplitude levels on the analog board using MH0026 driver amplifiers. The details of the analog circuitry are shown in Figures 3.6a, 3.6b, 3.6c and 3.6d. Various bias sources not located in RS-1 or RS-2 are also indicated. The use of S and T subscripts refers to storage and transfer gates respectively. For example, ϕ_{1S} and ϕ_{1T} are the two-phase clock applied to phase 1 storage and ϕ_1 transfer gates respectively. A physical description and operational details of the RSAM may be found in Reference [1].

(d) RS-1, RS-2 Bias Supplies

Details of the bias circuitry located in bins RS-1 and RS-2 are shown in Figures 3.7 and 3.8. Figure 3.9 identifies the bias controls at the front panels of RS-1 and RS-2. The DVM may be switched to any supply for either checking or setting purposes. Provision is made to remove power to the DVM when not being used to eliminate the noise encountered with these devices in operation.

Operational Results

The RSAM was operated as a synchronous recirculating correlator with a continuous input. The input signal was a repetitive pulse occurring at each loop cycle period. In Figure 3.4a the source strobe switch was set to "continuous," which grounds pin 1 of IC_3 making $\bar{S}_{1A}$ independent of $\overline{\text{GATE B}}$. Thus, with continuous $\bar{S}_{1A}$ strobe pulses input signal charge was added continuously to the signal charge already circulating in the loop. With this arrangement S_{1B} strobe pulses are still controlled by $\overline{\text{GATE B}}$, consequently trailing bias charges are only introduced during LOOP

CYCLE "O". By careful tuning of the input signal bias level, V_{G1A}, the dark current subtractor level, V_{DCS}, and using the procedure outlined in Reference [2] for evaluating signal-to-noise improvement a figure of 17 dB was obtained. This preliminary result compares favorably with the reported value of 17.5 dB [2].

An attempt was made to operate the RSAM at frequencies above 1 MHz. We found that the operation for the present system, even with fine tuning of the critical bias levels, was limited to about 2.5 MHz.

4. Interface Board

The purpose of the microprocessor/CCD interface board is to provide a flexible and easily reconfigurable high-speed interface between the microprocessor and the CCD modules. The interface board was designed to provide for transfer of data tables in memory directly to the CCD modules. The data tables are generated by the microprocessor during the initialization phase. A direct memory access controller, DMAC, has been incorporated to support this type of transfer. The reason for generating the data in the form of tables is that the CPU will not be able to do it in real time, but instead will serve the role as a system controller once an experiment is started.

The general structure of the board is divided into four functional blocks. These are: the DMA controller (and the Board Control Word), the bus interface logic which includes the simultaneous transfer logic, the two I/O ports and the high-speed FIFO buffer with its associated logic. Figure 4.1 illustrates the

general configuration of the interface board.

The DMAC is programmed by writing data into its control registers. One can select one of several functional modes. These are (1) search only, (2) sequential transfer, and (3) simultaneous transfer (some external logic is needed for this mode). Variables such as block length, transfer address, match pattern, interrupt generation, block/byte transfer, and cycle length are also under program control. The manner in which this is done and the functional description of the DMAC hardware are contained in the technical literature provided by Zilog on the DMA.

The high-speed transfer logic is located on the board and extensive signal buffering is needed towards the system bus. Some signals are bidirectional and, hence, we have used bidirectional buffers. The fact that both the CPU and the DMAC can be bus master complicates the logic controlling the buffer direction.

In the case of simultaneous DMA transfer, which is programmed in search only, a write signal is created at the same time as memory read is generated, so that the actual transfer is taking place in the same cycle. Thus, simultaneous transfer increases the transfer rate by a factor of two. At this time, the DMAC is the bus master and, hence, the bus interface logic will turn the buffer accordingly.

To make the interface circuitry as flexible as possible, necessary changes in the hardware when changing transfer mode and direction is also under software control. For this purpose, a control word, called the Board Control Word (BCW), has been

established, which the CPU can write to as well as read from.

There are two I/O ports on the board. One of them is an ordinary bidirectional I/O port covering four I/O addresses. This port is to be used for control signalling. The other is a special purpose write only port, that we call the parallel port. It has the following features. It can be either transparent or latched, the selection being made via the BCW. It can also be addressed in an ordinary fashion or selected as a simultaneous port by means of the BCW.

The FIFO buffer is intended to provide the signal generator with data and handshaking signals to the DMAC. Its presence provides for a minimal software overhead during operation. The surrounding logic is needed for synchronization and for warning the DMAC that the FIFO is nearly empty.

Besides the abovementioned blocks, address-decoding logic is also present on the board to decode the 32 I/O addresses dedicated to the interface board. Below is one example of how the function of the interface board can be set up.

- The CPU loads the DMAC with commands and addresses, activates the required hardware function by writing to the BCW and then enables the DMAC.
- The DMAC requests the system bus for starting a transfer to the FIFO buffer, for instance. When the FIFO is filled the DMAC will sense this and return the bus to the CPU, only to request it again when the FIFO needs more data.
- The CPU can now do some calculations, transfers or general

control of the experiment. Alternatively, the CPU can reprogram the DMAC to perform a different transfer while it is waiting for the FIFO flag signal for reloading. The timing requirements during this flip-flop type of action are very sensitive, and errors can easily occur if caution is not taken.

The Board Control Word (BCW)

The BCW provides a method for changing the hardware function unde software control. Besides being writable it can also be read by the CPU which is useful for debugging and makes it unnecessary to keep a copy in a memory location. Some bits of the BCW determine the data flow while some others are controlling the output ports to enable several of them to be tied together in order to minimize the use of wires on the system bus. The BCW format and bit definition are as follows:

S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

S_7: A "1" will enable the simultaneous logic. NOTE: The DMAC has to be disabled before changing this bit; also, before re-enabling, the DMAC has to be programmed for simultaneous transfer.

S_6: A "0" will connect the DMAC ready pin to the FIFO buffer logic. A "1" will connect the DMAC ready pin to the parallel port. In both cases will ready active,

i.e., low, enable the DMAC to resume transfer in the burst mode.

S_5: Not yet used.

S_4: A "1" will be one of the conditions to enable the output of the parallel port.

S_3: A "1" means 8-bit correlation, and is also another condition to enable the parallel port. A "0" means 1-bit correlation. This bit and the following was originally defined to be used in conjunction with the ABC CCD device. Some kind of redefinition will take place in the future.

S_2: A "1" will connect (enable) the parallel port to the correlator. A "0" will connect a skewed version of the test signal to the correlator (ABC).

S_1: Not yet used.

S_0: A "1" will allow the parallel port to be transparent during simultaneous transfer, while a "0" will cause it to be latched.

Address Map

The Z-80 microprocessor has an I/O addressing range of 00_H - FF_H* (256 distinct addresses) of which some already are reserved at system level. The MCB board (where the CPU is located) has already decided the address space $C0_H$ - CF_H (a total of 32) as follows:

---

*H stands for hex, i.e., the base of the numbers is 16.

MDC: CF_H - $D3_H$

CTC: $D4_H$ - $D7_H$

PIO: $D8_H$ - DB_H

USART: DC_H - DF_H

Not used: CO_H - CE_H

This means that the available address space is OO_H - BF_H and EO_H - FF_H where we choose to reserve the latter 32 addresses for the interface board in the following manner.

Eight I/O groups were defined to correspond to specific types of devices and ports. Then four subgroups enable each I/O group to respond to and serve four local addresses.

I/O Group	Address Group	Function/device supported
Y_0:	EO_H - $E3_H$	DMAC
Y_1:	$E4_H$ - $E7_H$	Control, status
Y_2:	$E8_H$ - EB_H	FIFO buffer
Y_3:	EC_H - EF_H	Parallel port
Y_4:	FO_H - $F3_H$	I/O port
Y_5:	$F4_H$ - $F7_H$	Clock rate
Y_6:	$F8_H$ - FB_H	Correlation skew
Y_7:	FC_H - FF_H	Software controlled resets

Subgroup

X_0: -

X_1: -

X_2: -

X_3: -

X_4: 0 4 8 C

X_5: 1 5 9 D

X_6: 2 6 A E

X_7: 3 7 B F

As an examp'e of how to use this decoding scheme the following is the way in which it is used at the present.

	Address
DMAC 1	$Y_0 \cdot X_7 = E3_H$
BCW	$Y_1 \cdot X_7 = E7_H$
FIFO 1	$Y_2 \cdot X_7 = E8_H$
Parallel port 1	$Y_3 \cdot X_7 = EF_H$
I/O port - signal generator mode	$Y_4 \cdot X_7 = F3_H$
I/O port - PTF mode	Y_5
Software Reset	$Y_7 \cdot X_6 = FE_H$
Software Master Reset	$Y_7 \cdot X_7 = FF_H$

5. Projections

A portion of the circuitry for the programmable transversal filter (PTF) has been completed. The remainder will be completed over the next six months. There is a difficulty encountered in loading the coefficients of the PTF. The problem has not been fully resolved, since there is no satisfactory way of ascertaining successful coefficient loading directly. Further attention will be devoted to this problem.

The circuitry for the analog-binary correlator (ABC) is designed and construction is now under way. The control circuitry that ties the ABC to the interface board is being designed. The design of the two-dimensional module is also under way.

Software will be developed as needed to test out the modules.

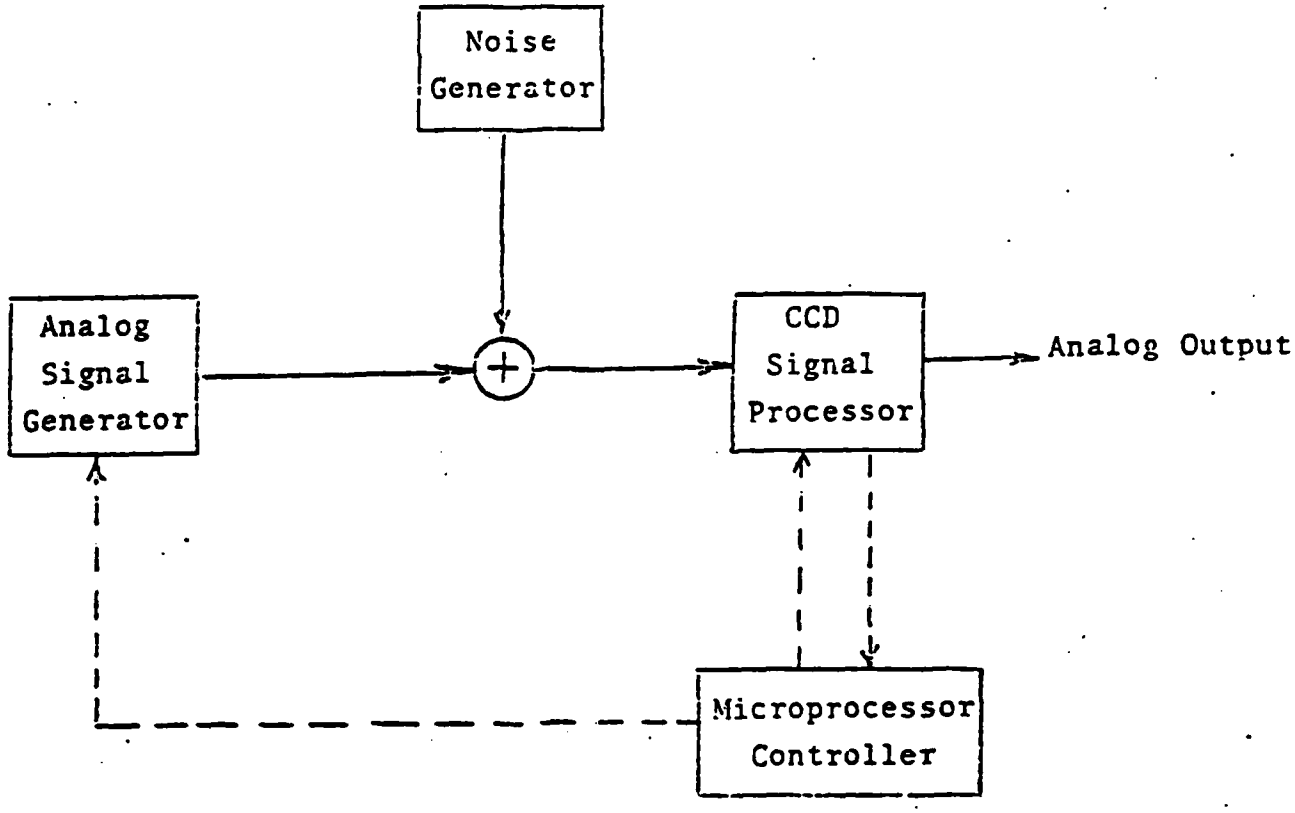

Figure 1.1 General Configuration of Sampled-Analog Signal Processing Module

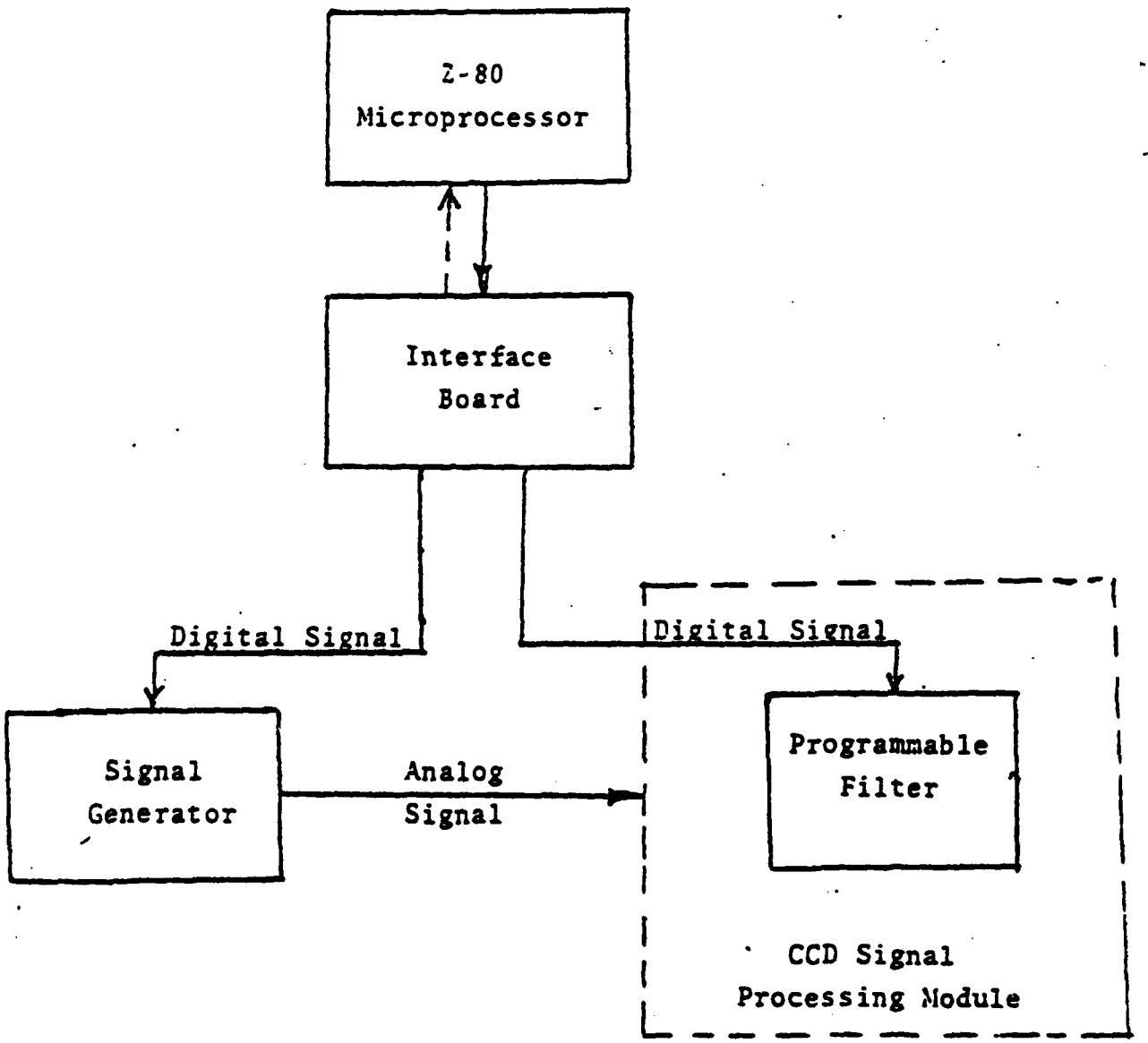

Figure 1.2 Functional Block Diagram of Signal Processing System with the Interface Board

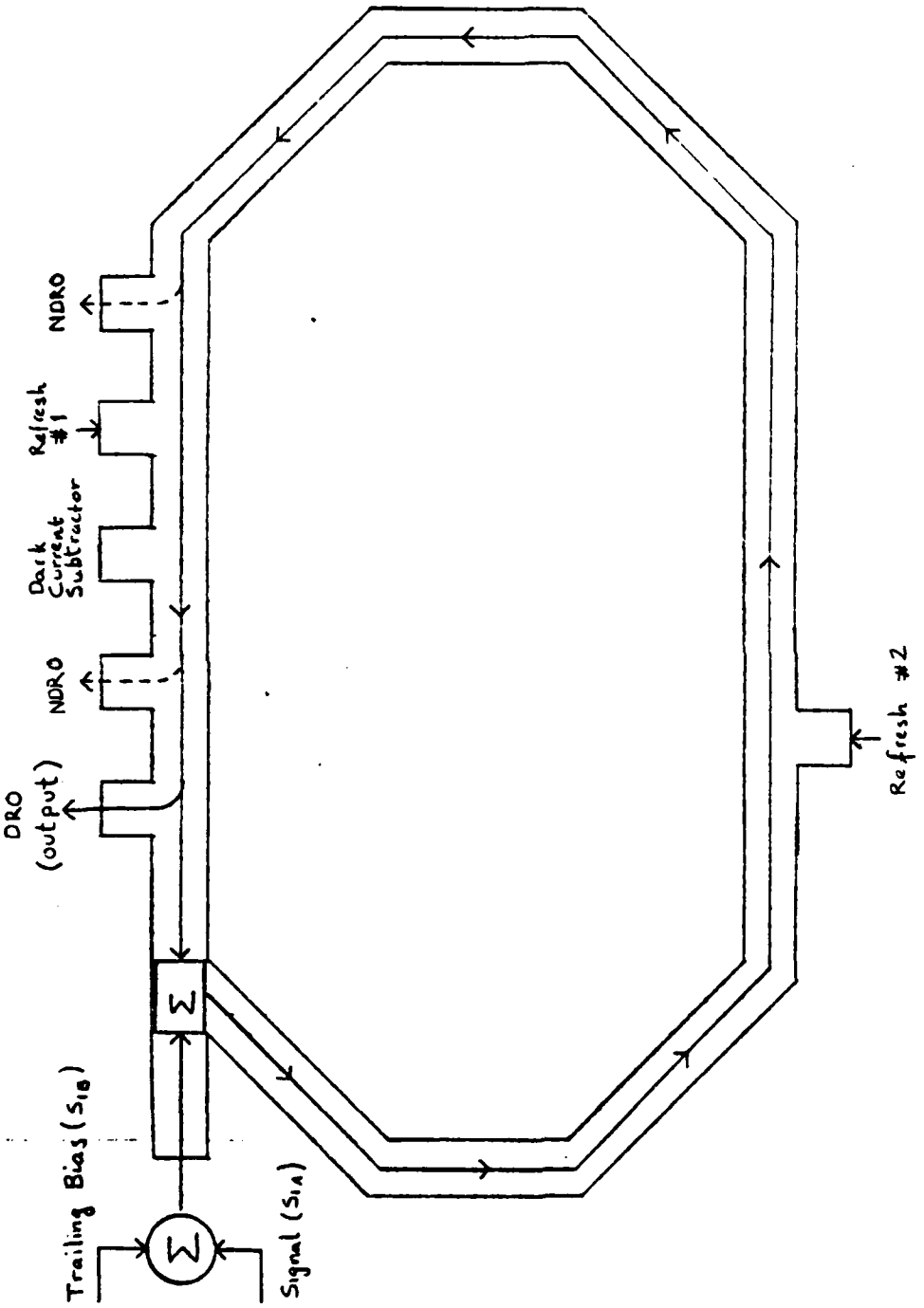

Figure 3.1 Schematic representation of 1024 stage CCD loop. 256 stage CCD loop contains only a signle refresh stage.

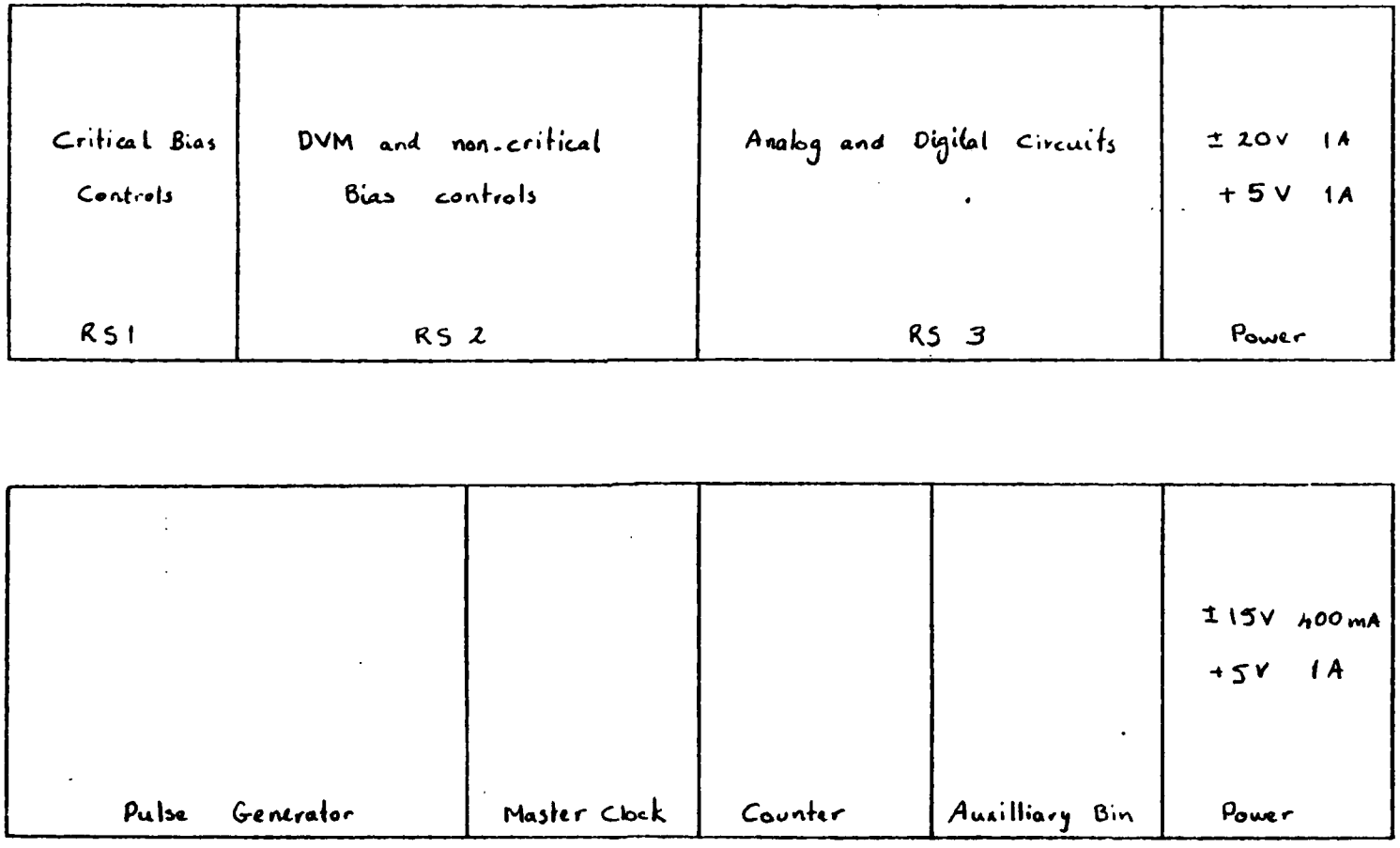

Figure 3.2 Modular arrangement of RSAM and support circuitry using two TM 506 power modules.

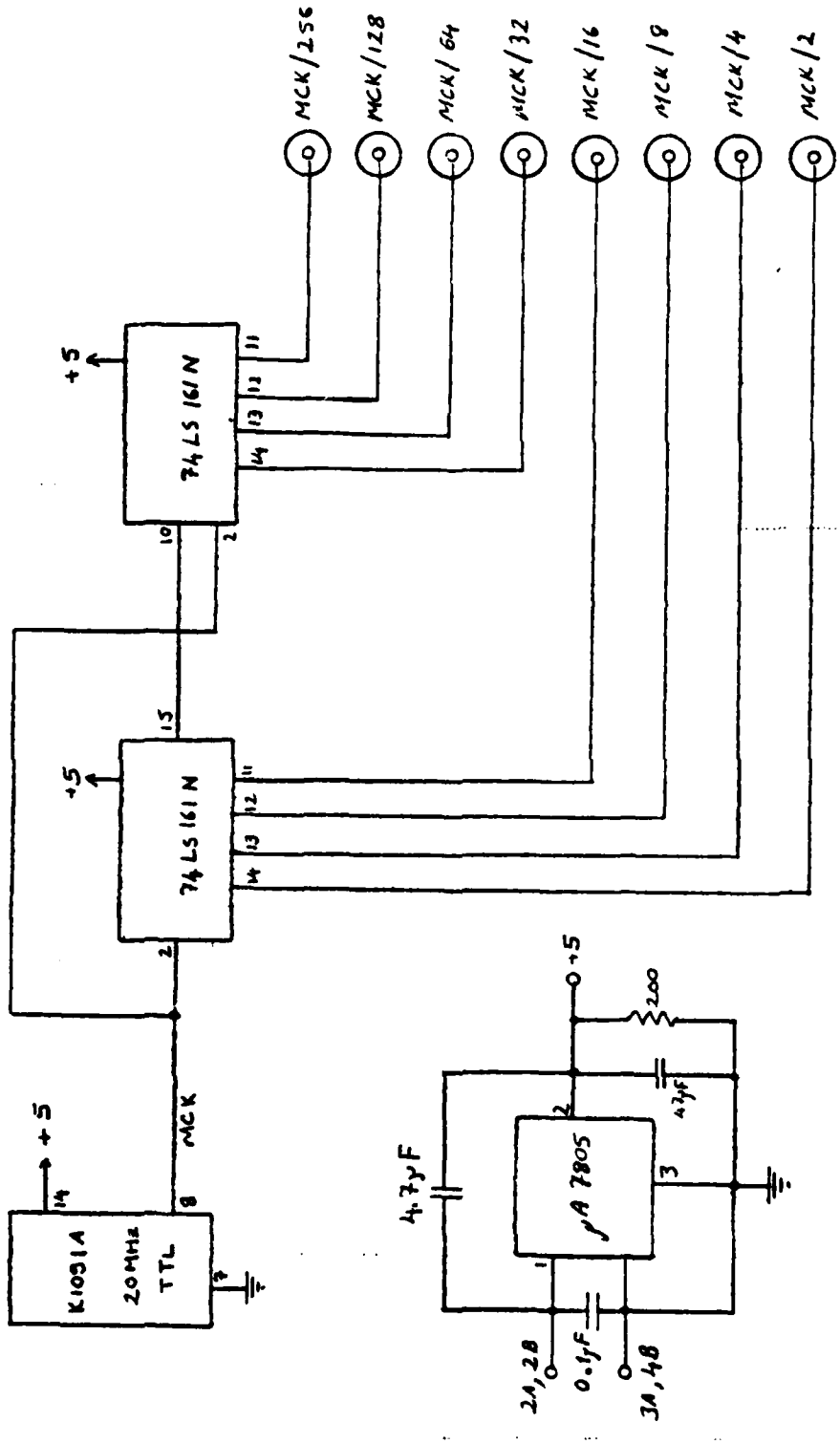

Figure 3.3 Master clock circuitry (MCK).

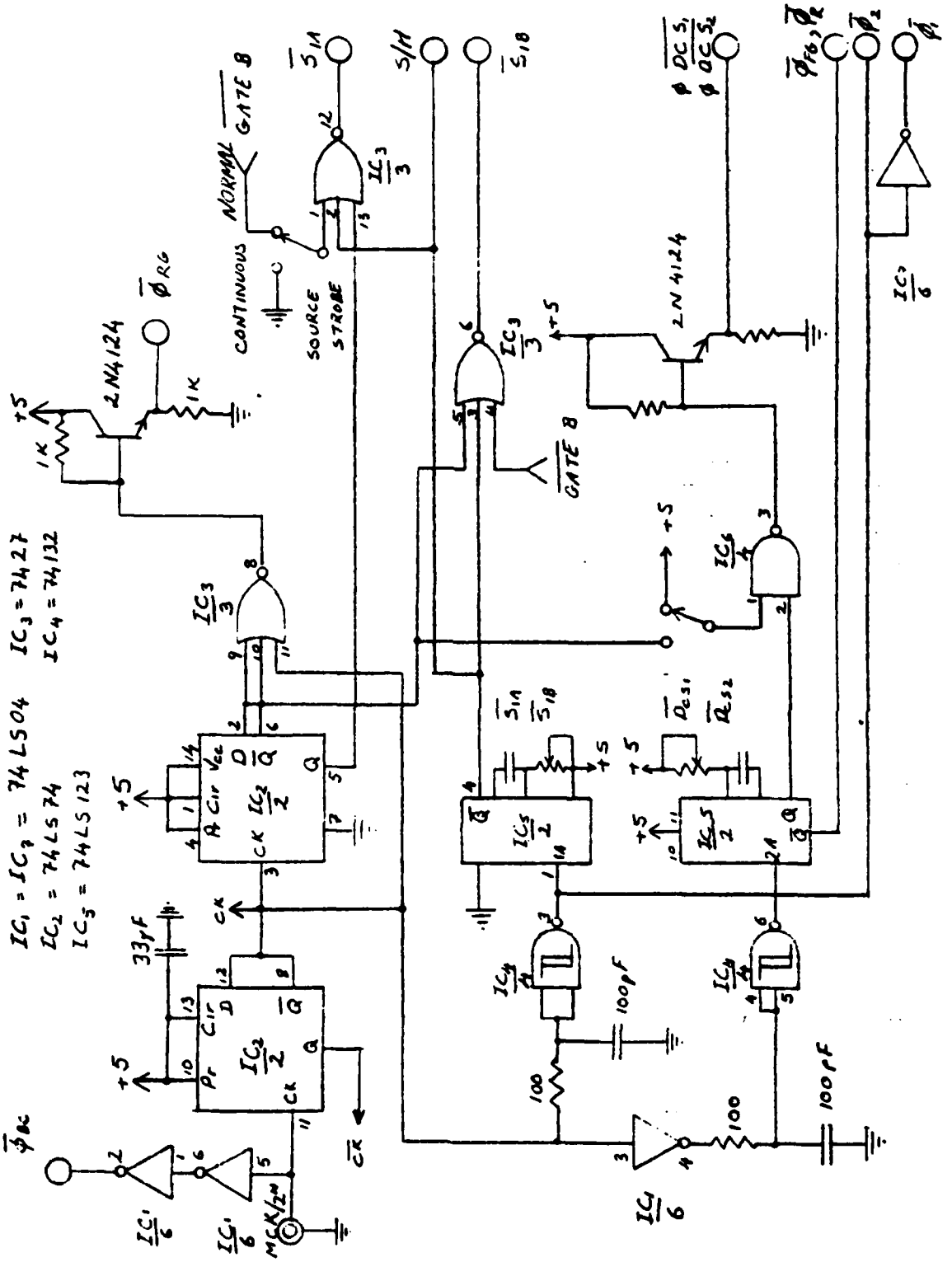

Figure 3.4a RS-3 digital board circuitry.

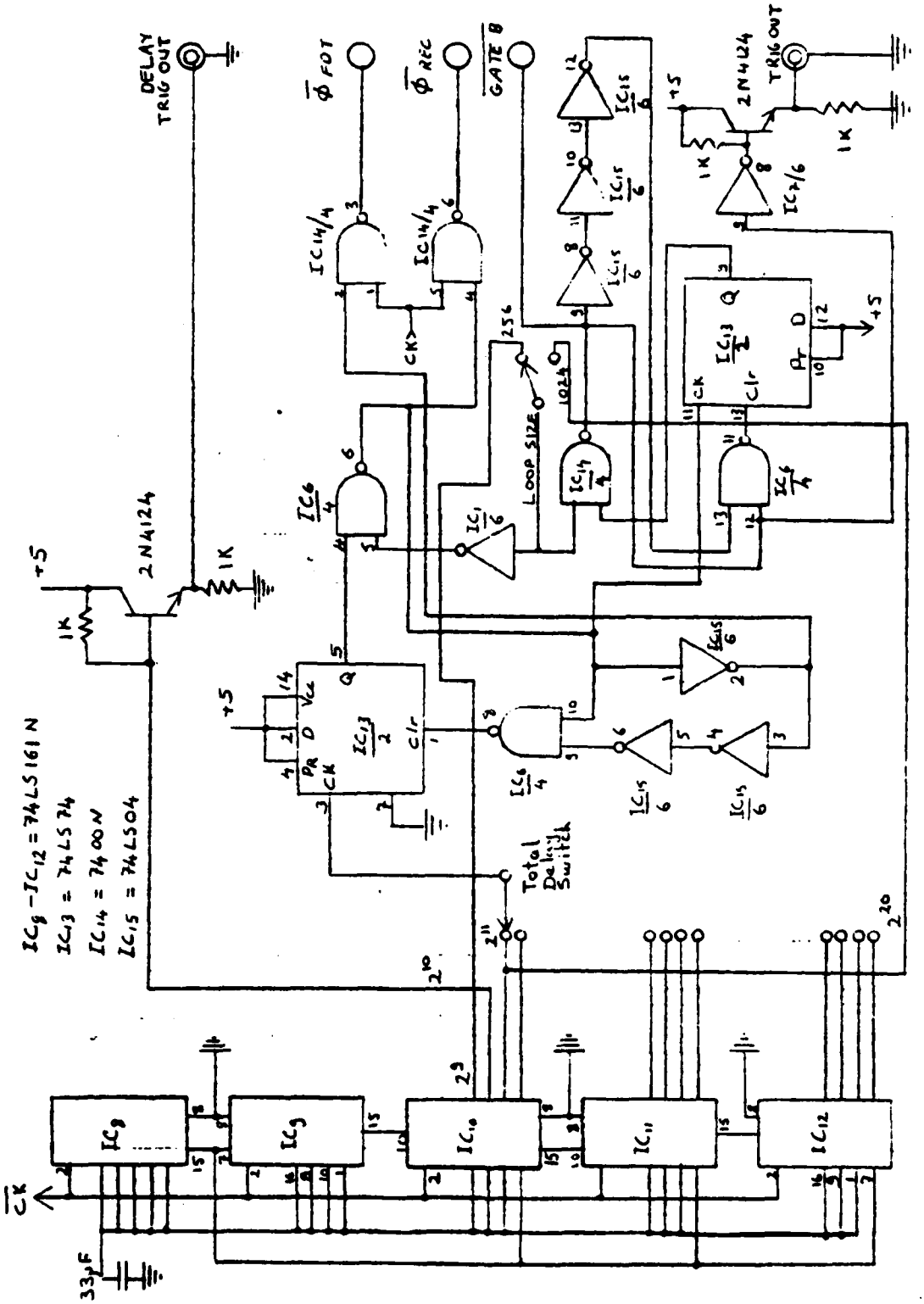

Figure 3.4b RS-3 digital board circuitry (continued).

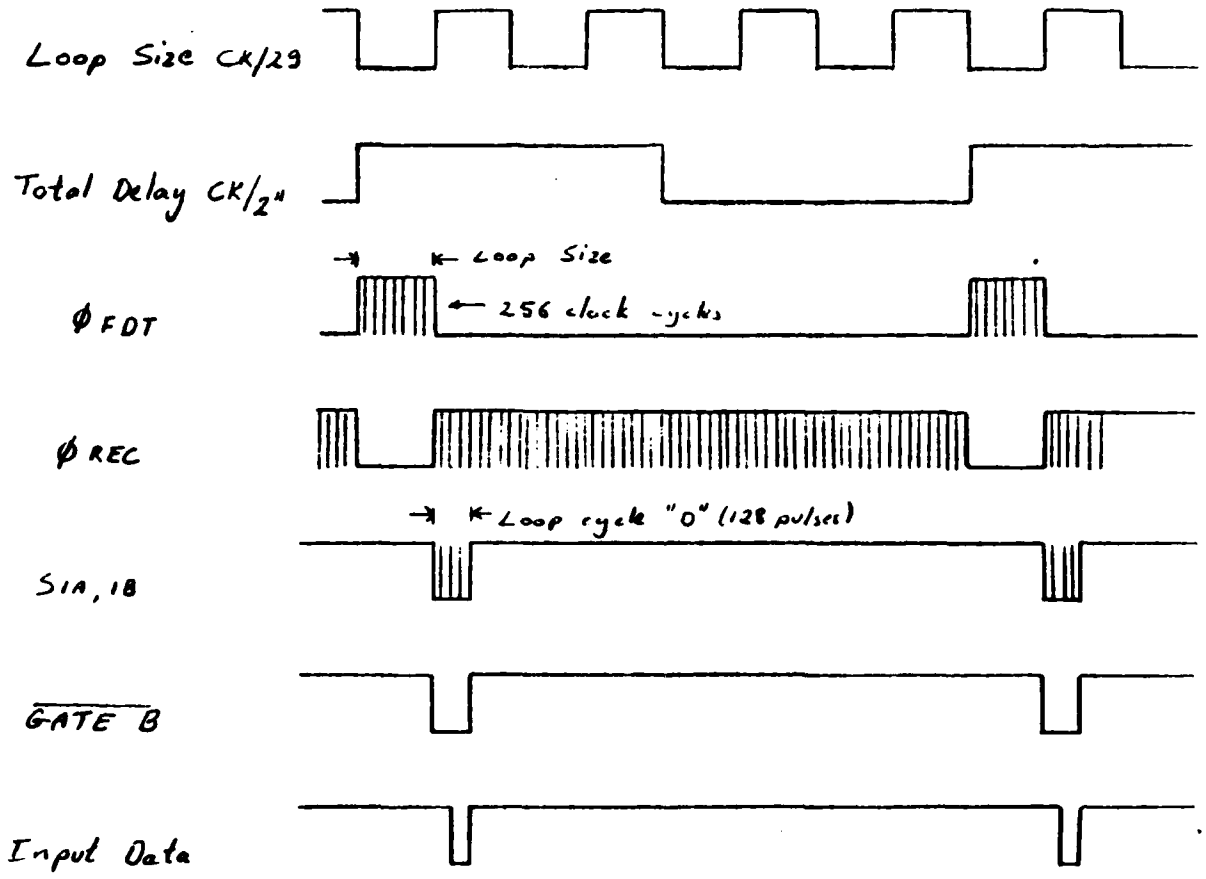

Figure 3.5 Simplified timing diagram for the 256-stage closed-loop CCD.

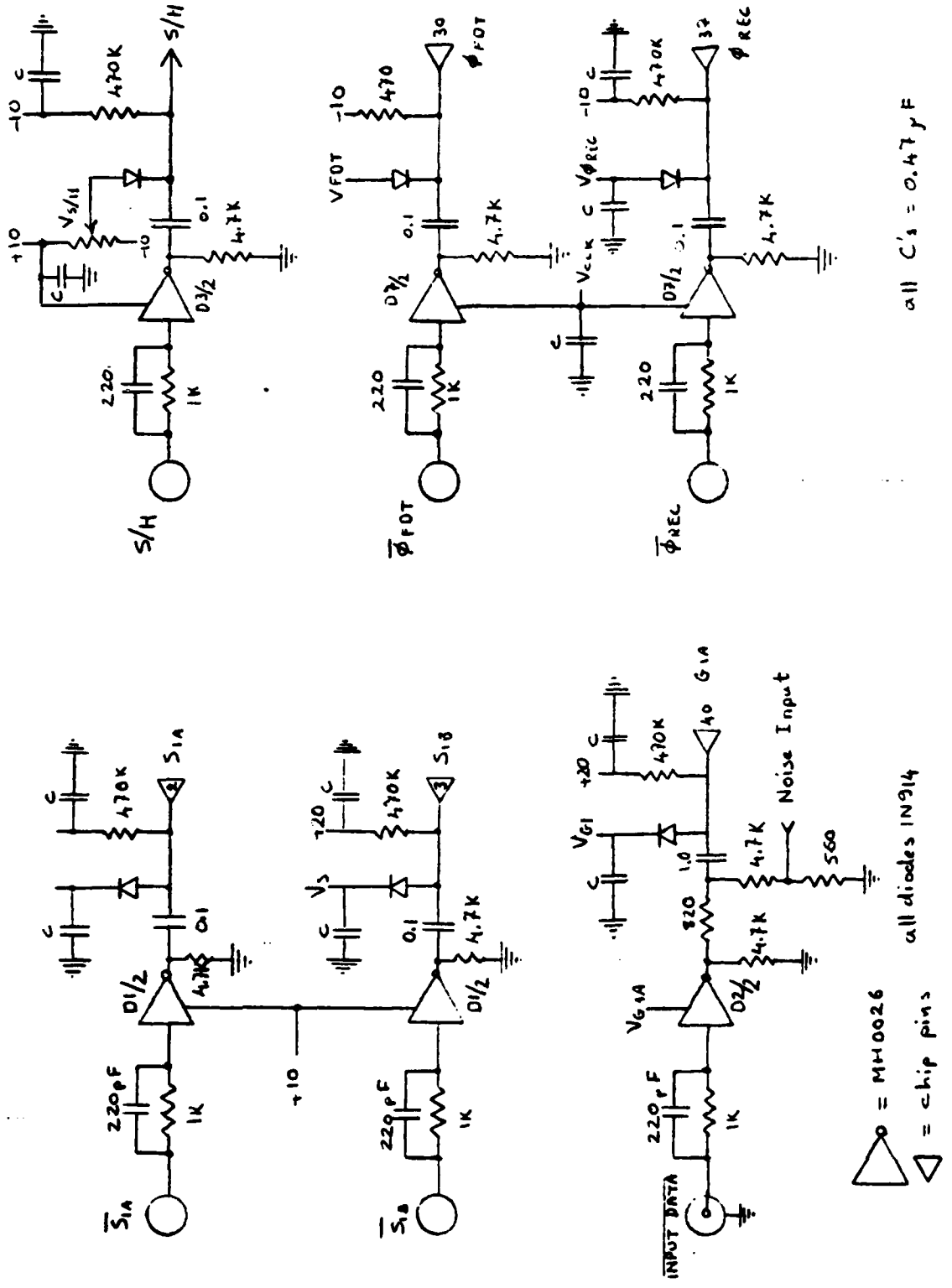

Figure 3.6a RS-3 Analog board circuitry.

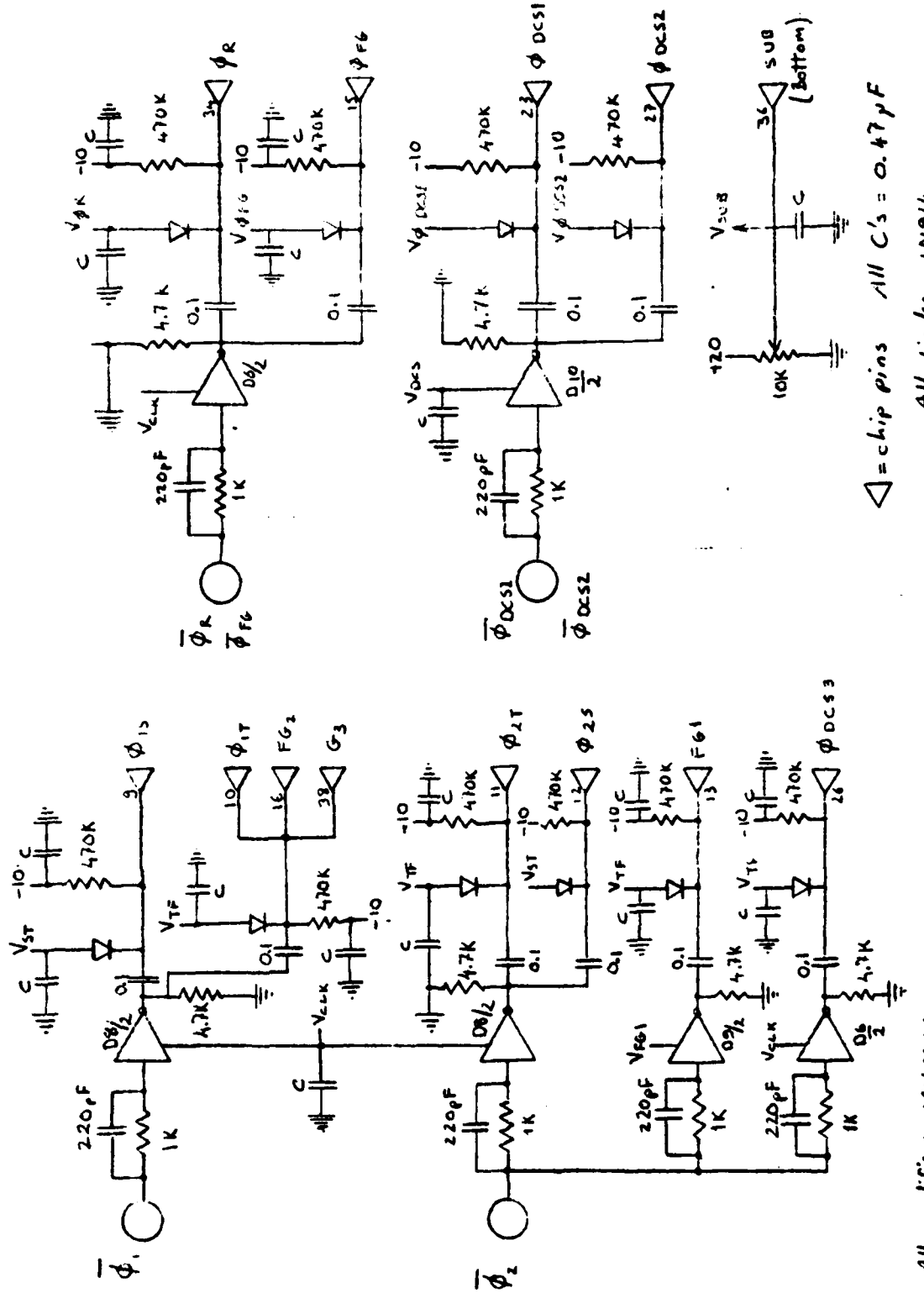

Figure 3.6b RS-3 Analog board circuitry (continued)

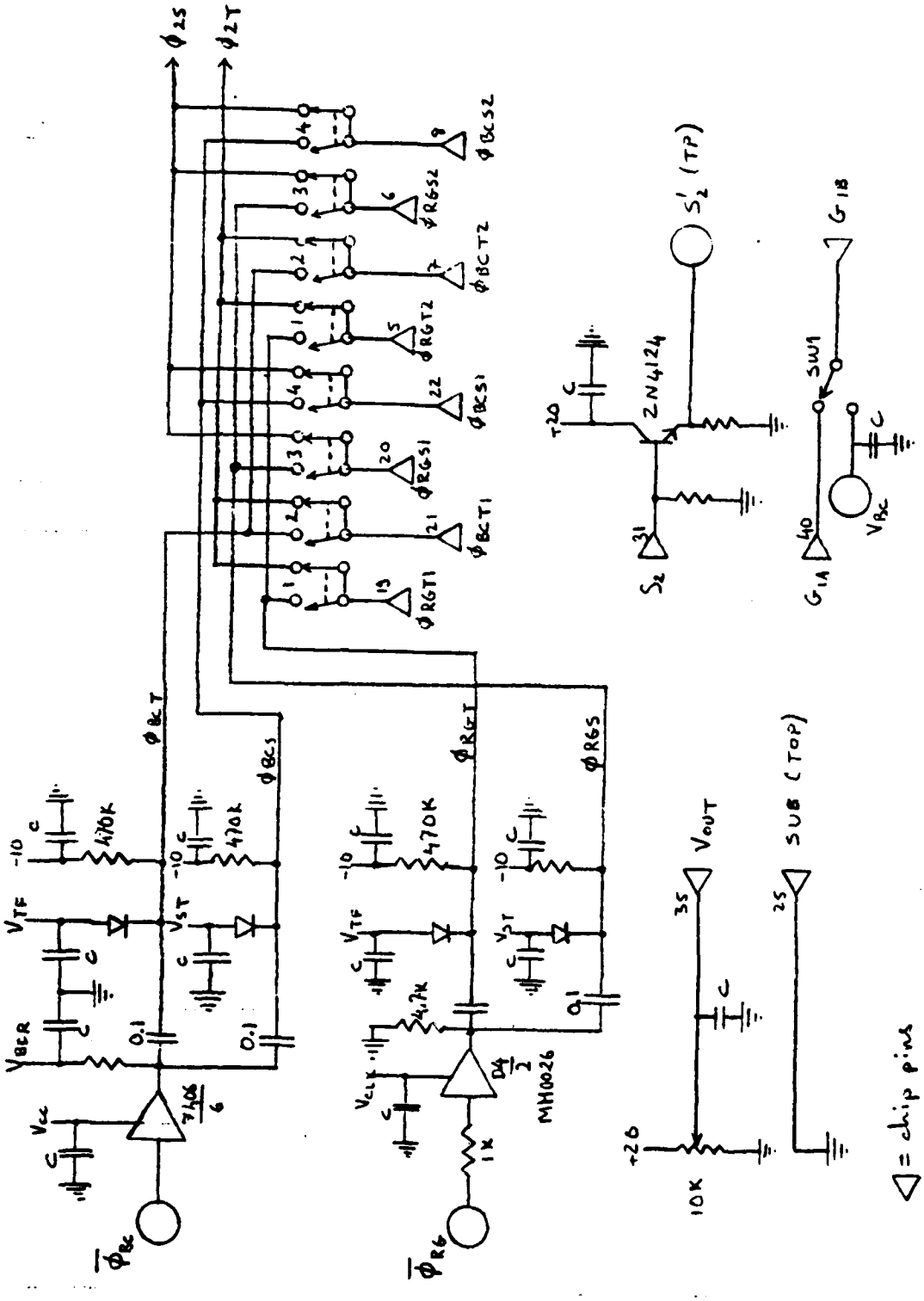

Figure 3.6c RS-3 Analog board circuitry (continued)

△ = chip pins
all C's = 0.47μF

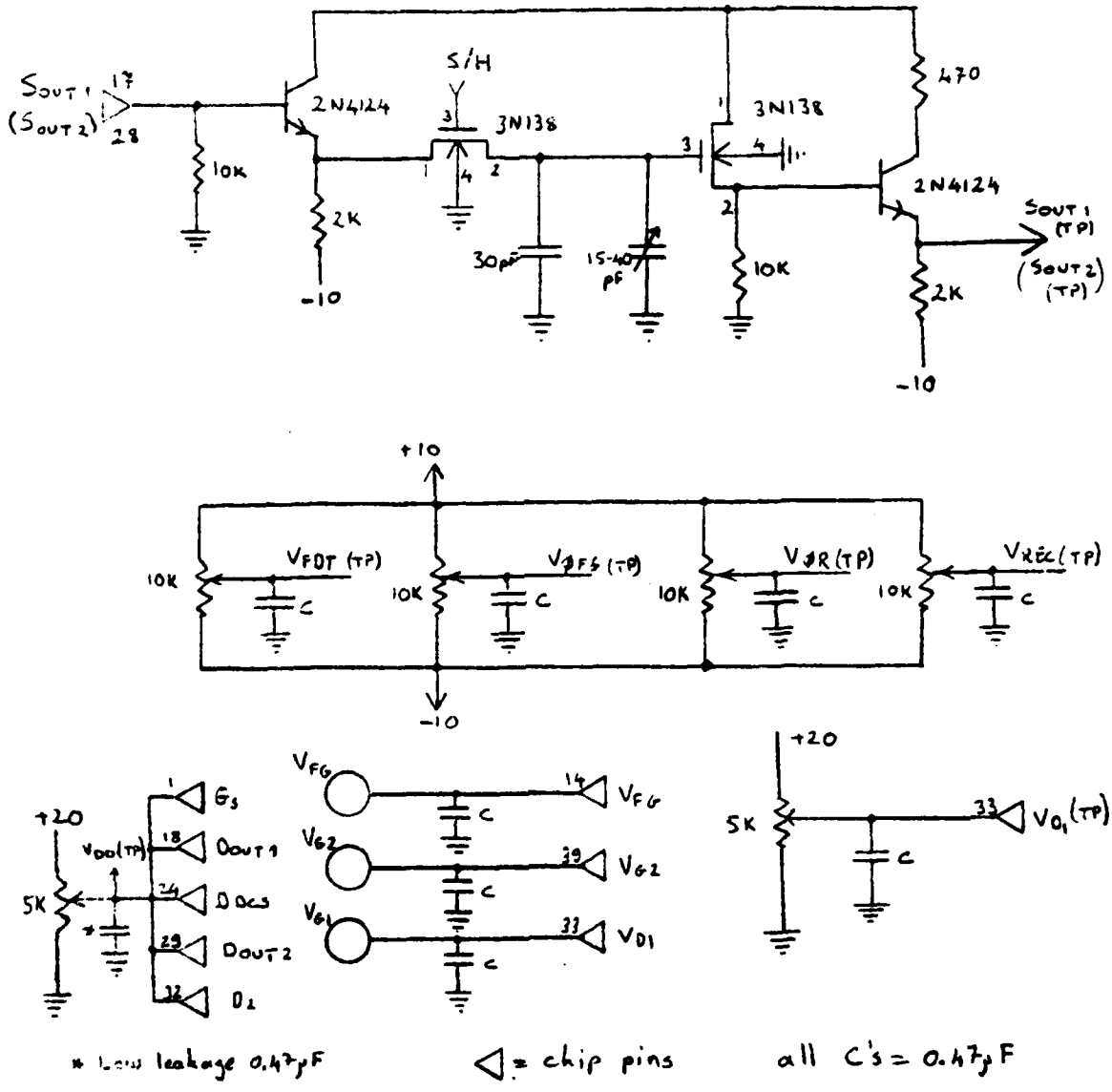

Figure 3.6d RS-3 Analog board circuitry (concluded)

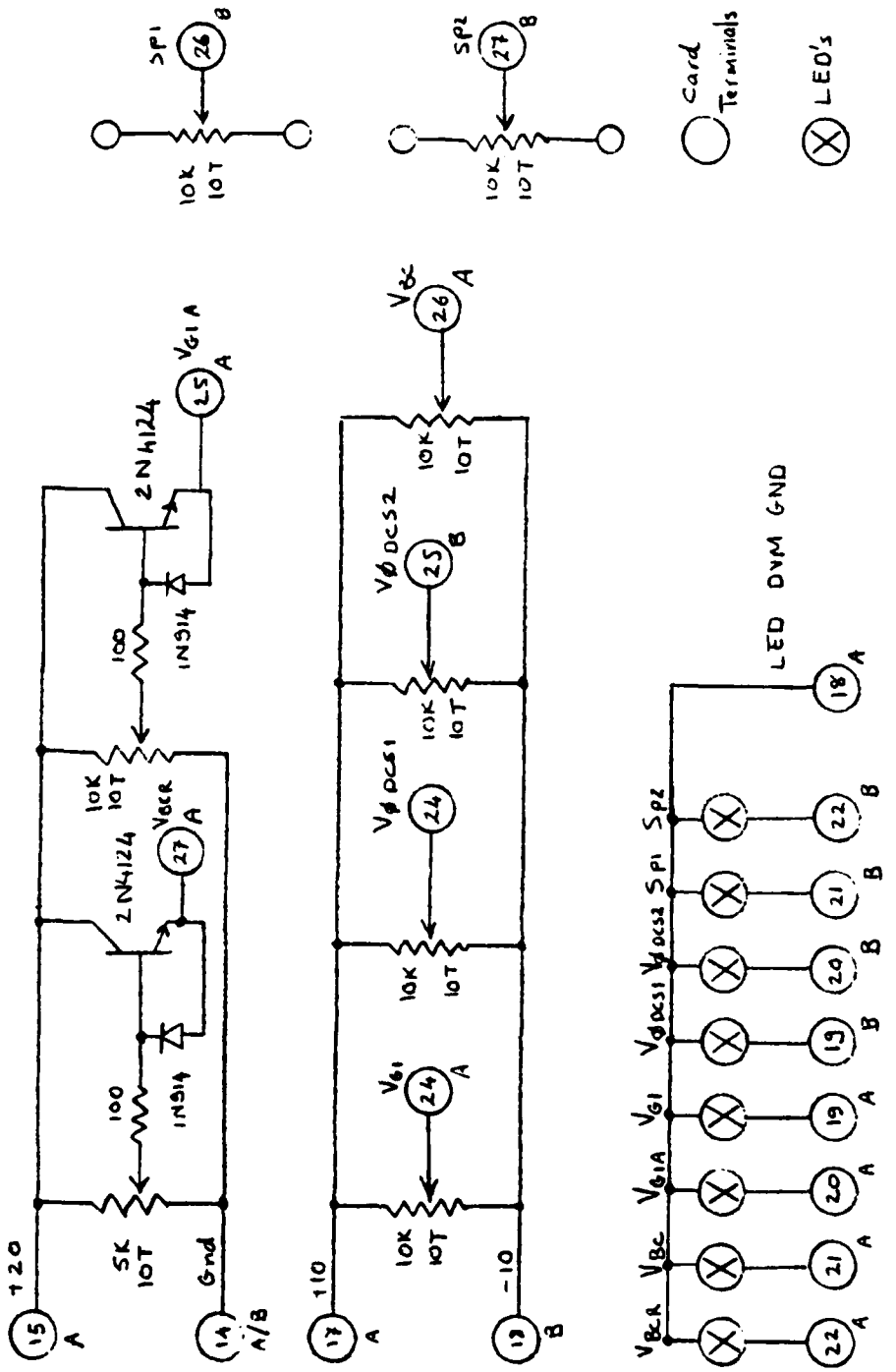

Figure 3.7 RS-1 bias circuitry.

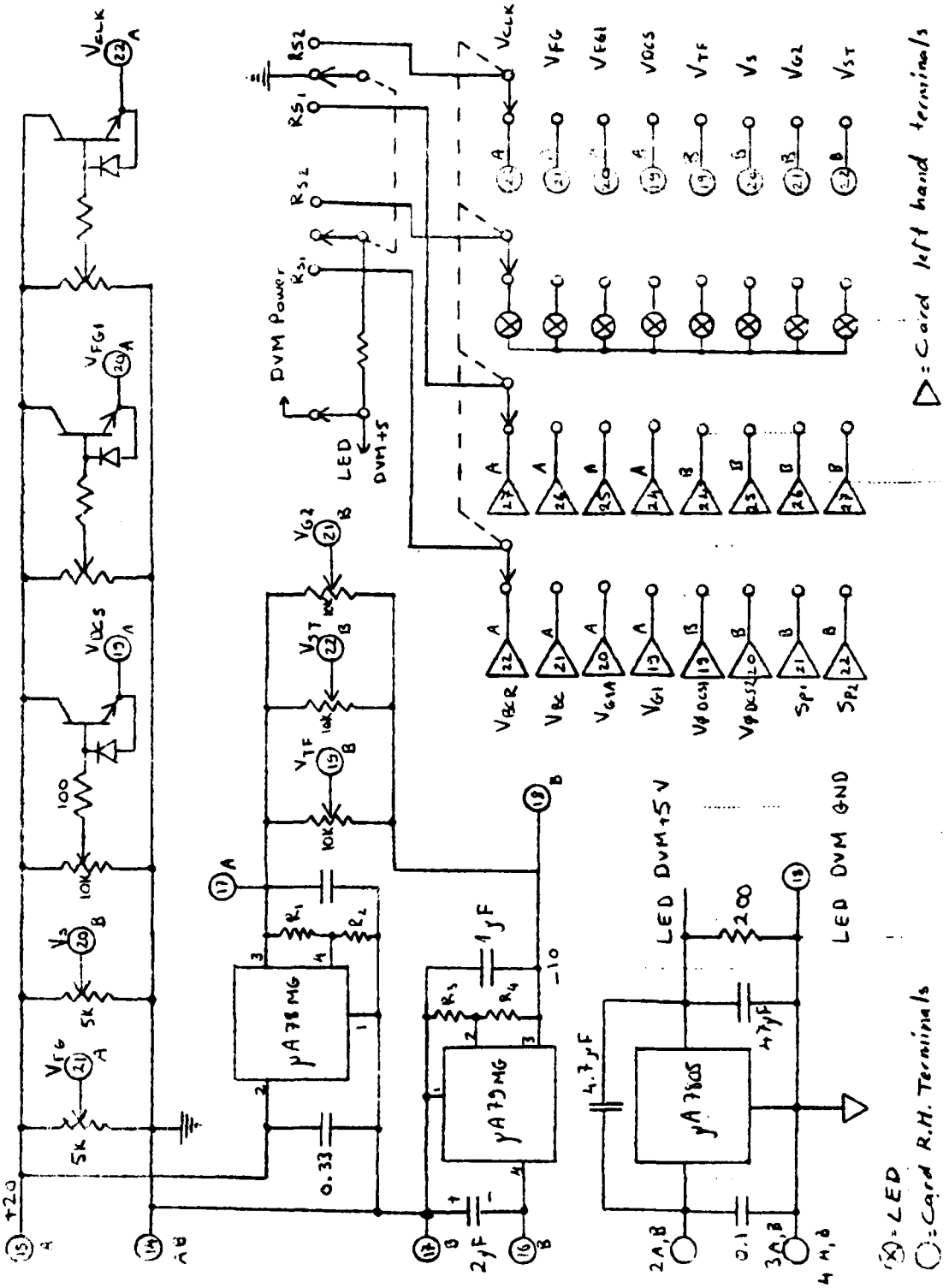

Figure 3.8 RS-2 bias circuitry.

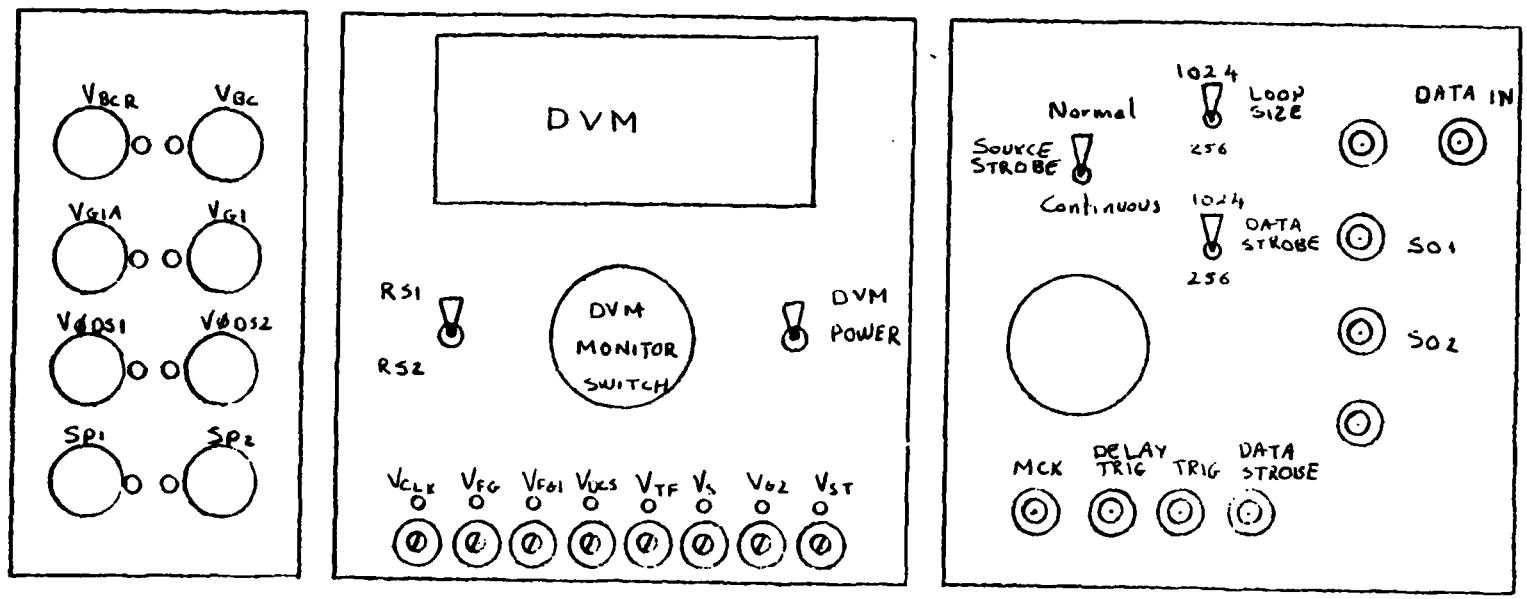

Figure 3.9 Front panel layout for RS-1, RS-2 and RS-3.

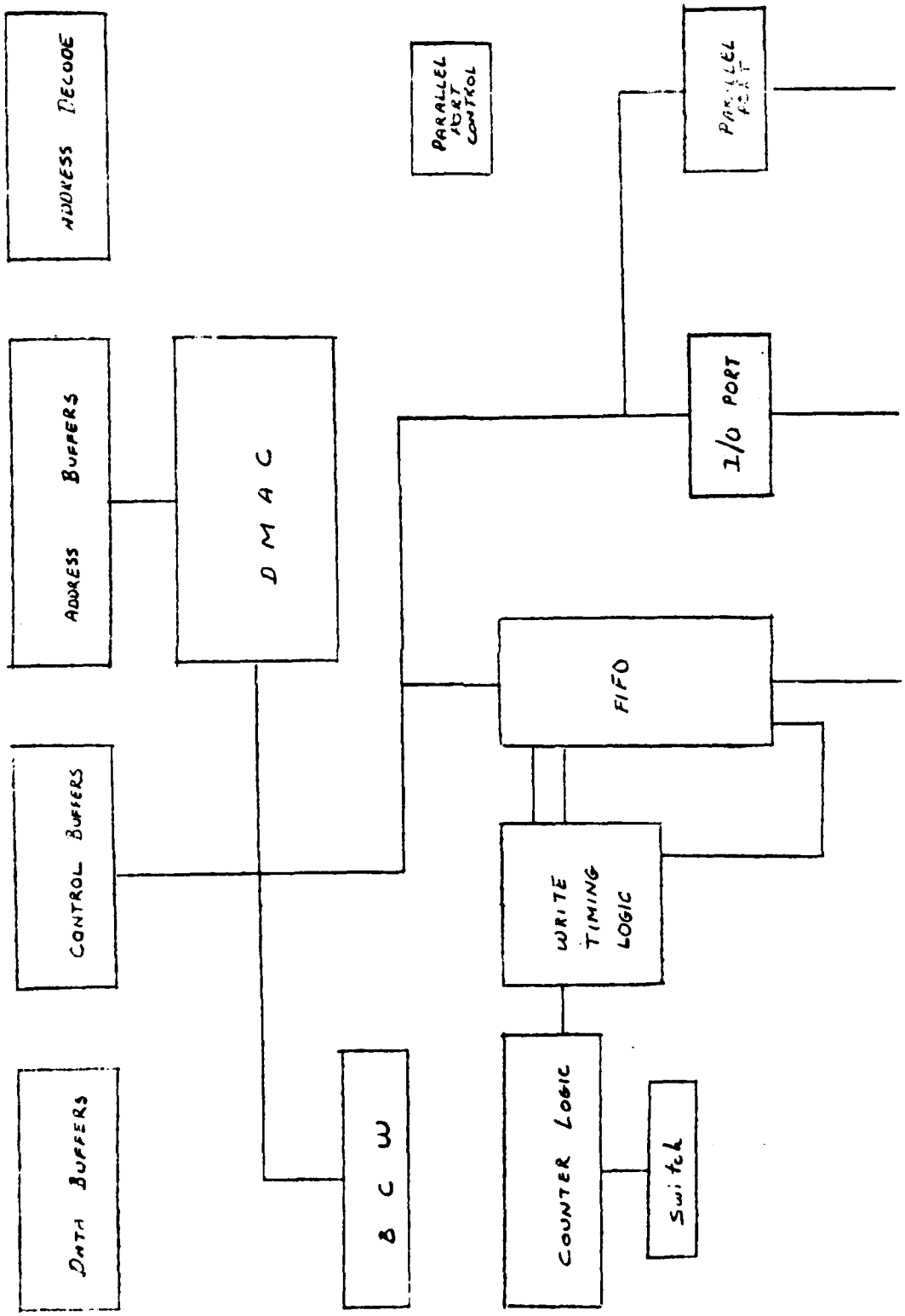

Figure 4.1 Block diagram of microprocessor interface board.

References

[1] W. F. Kosonocky, D. J. Sauer, "CCD long-time delay line," Interim Report RADC-TR-78-236, November 1978.

[2] W. F. Kosonocky, D. J. Sauer, C. Y. Tayag, F. V. Shallcross, "Low-loss charge-coupled device," Final Report RADC-TR-79-144 June 1979.

END

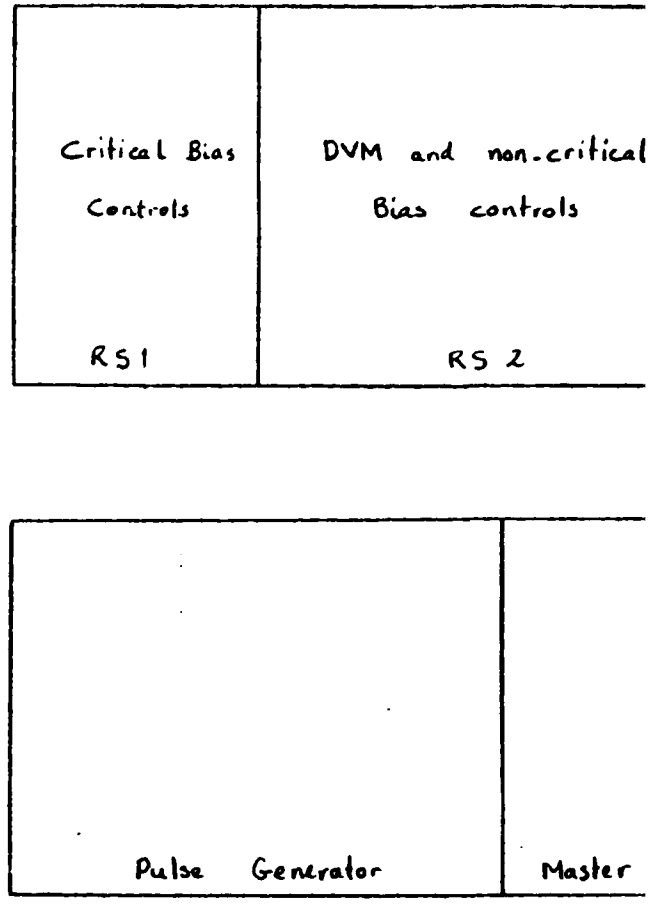

Figure 3.2 Modular arra
using two TM